REMARKS

In the Advisory Action mailed July 12, 2005, the rejection of the claims under under 35 USC §102(b) as being anticipated by Akao et al. (US Patent 5,307,464, hereinafter "Akao") has been withdrawn. Applicant gratefully acknowledges the withdrawal of the rejection under 35 USC §102(b).

Claims 1-6, 10-13, 23 and 28 remain rejected under 35 USC §103(a) as being obvious over "The Programmable Logic Data Book 2000" in view of Akao. Finally, claims 3, 11-13, 24-27 and 29-32 remain rejected under 35 USC §103(a) as being obvious over Akao (or "The Programmable Logic Data Book 2000" and Akao) in view of Applicant's disclosure in Paragraphs [0015] and [0016].

In response to the rejection of claims, Applicant has amended the claims to distinguish over the references. In particular, Applicant has amended each of the independent claims 1, 23 and 29 to recite "an input/output block coupled to said programmable routing matrix, wherein said programmable routing matrix provides input/output routing" for the configurable peripheral device (or specifically the universal asynchronous receiver transmitter of claim 29) by way of the input/output block "without using a sub-processor." Applicant respectfully submits that the claims as amended distinguish over any combination of the references.

I. Independent Claims 1 and 6

In response to the rejection of claims 1-6, 10-13, 23 and 28 as being obvious "The Programmable Logic Data Book 2000" in view of Akao, Applicant respectfully submit that independent claims 1 and 6 as amended clearly distinguish over the references. Applicant respectfully reiterates that neither reference discloses or suggests "a bus coupled between said processor core and said configurable peripheral device, said bus connecting said processor core and said configurable peripheral device without using a sub-processor." While "The Programmable Logic Data Book 2000" fails to disclose a processor (and therefore fails to disclose a bus coupled to a processor core as claimed), Akao fails to disclose or suggest a bus connected between a processor core and a configurable peripheral device without using a sub-processor. It is suggested in the Office Action that Akao discloses a bus

connecting the processor core 2 and a configurable device without a sub-processor in the embodiment where a PLA or PLD is implemented in place of sub-processor 5 as disclosed in col. 32, lines 23-30 and col. 33, lines 46-58. However, Applicant reiterate that col. 32, lines 23-30 and col. 33, lines 46-58 of Akao fail to disclose or suggest that a PLA or PLD is used in place of sub-processor 5. Col. 32, lines 23-30 of Akao states that operation control signals "can also be generated by a wired logic configuration utilizing PLDs [or] PLAS." Similarly, col. 33, lines 46-58, indicates that the scope of the invention is not limited to such a sub-processor, but that "[i]nstead, a programmable logic array can also be configured by using non-volatile memory elements." Applicant respectfully submits that there is no teaching or suggestion that a PLD or PLA is coupled to a processor core without using a sub-processor.

However, Applicant has further amended the claims to more clearly distinguish over the references. Applicant respectfully submits that neither reference discloses or suggests "an input/output block coupled to said programmable routing matrix, wherein said programmable routing matrix provides input/output routing for said configurable peripheral device by way of said input/output block without using a sub-processor." Applicant respectfully submits that the references could not be properly combined in view of the amendments, and any combination of the references would not lead to Applicant's claims. That is, Akao teaches away from an input/output block coupled to the programmable routing matrix, wherein the programmable routing matrix provides input/output routing for the configurable peripheral device by way of the input/output block without using a sub-processor. In particular, Akao discloses the use of two input/output ports. A first input/output port 6 shown in Fig. 1 of Akao enables the operation of the device in a single chip mode or an external extended mode based upon a mode signal EPM. The input/output port 6 is connected to the external pin group "a" which is used as an interface between the microprocessor 1 and external hardware. The input/output port 6 includes an internal data direction register and an internal data register. The data direction register, which receives the data from the CPU 2, is used for holding data determining the direction of data input or output through the external pin group "a." In order to write data into the data direction register, the CPU 2 asserts an address assigned to the data direction register on the

address bus 7, outputting the data through the data bus 8. A write control signal asserting on the control bus 11 then transfers the data into the data direction register. In the single chip mode, the external pin group comprises data input, data output and data input/output pins. In the externally extended mode, the external pin group "a" also includes address output pins in addition to the data input, data output and data input/output pins. (Col. 12, lines 10-29).

However, when the sub-processor 5 implements peripheral functions, a flag unit 17 is connected directly to the external pin group 10. (Col. 22, lines 44-53). While the sub-processor 5 may receive external data to be loaded in MicroROM (EPROM) 13 or may provide results to the CPU by way of the buses 7, 8 and 11, there is no teaching or suggestion of an input/output block coupled to the programmable routing matrix that provides input/output routing for a configurable peripheral device by way of the input/output block without using a sub-processor as claimed. In contrast, Akao specifically teaches that any external communication for peripheral functions is by way of the external pin group 10 using a sub-processor. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). More importantly, if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Similarly, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). Applicant respectfully submits that Akao and "The Programmable Logic Data Book 2000" are not properly combined.

Further, even if the references could be combined, any combination of Akao

and "The Programmable Logic Data Book 2000" would not lead to Applicant's claims. That is, neither reference, alone or in combination, discloses (i) a bus coupled between the processor core and the configurable peripheral devices, wherein the bus connects the processor core and the configurable peripheral device without using a sub-processor, or (ii) an input/output block coupled to the programmable routing matrix, wherein the programmable routing matrix provides input/output routing for the configurable peripheral device by way of the input/output block without using a sub-processor. Applicant respectfully requests reconsideration of the rejection of independent claims 1 and 6 in view of the amendments and remarks.

II. Independent Claim 29

Applicant respectfully submits that independent claim 29 is allowable over Akao (or any combination of "The Programmable Logic Data Book 2000" and Akao) in view of Applicant's Paragraphs 15-16 for the same reasons set forth above with respect to independent claim 1. While claim 29 is directed to an integrated circuit specifically comprising a universal asynchronous receiver transceiver circuit implemented in programmable logic, the combination of references fails to disclose or suggest a bus coupled between a processor core and a universal asynchronous receiver transmitter circuit, or an input/output block coupled to a programmable routing matrix, for the same reasons set forth above with respect to claims 1 and 6. Applicant has further corrected an antecedent basis error by changing "configurable peripheral device" to "universal asynchronous receiver transmitter." While Applicant's Paragraphs 15-16 is cited for disclosing basic functions of a UART, Applicant's Paragraphs 15-16 fail to disclose or suggest the subject matter of independent claim 29 which are not disclosed by "The Programmable Logic Data Book 2000" or Akao. Accordingly, Applicant respectfully requests reconsideration of the rejection of independent claim 29 in view of the amendments and remarks.

III. Dependent Claims

Applicant respectfully submits that the dependent claims 2-6, 10-13, 22-28 and 30-32 are allowable over any combination of "The Programmable Logic Data Book

2000" and Akao or Applicant's Paragraphs 15-16 for the same reasons that the independent claims are believed allowable.

IV. Conclusion

All claims should be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 24, 2005.

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